AUTOMATIC GENERATION OF HARDWARE DESCRIPTION LANGUAGE CODE FOR COMPLEX POLYNOMIAL FUNCTIONS

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ABSTRACT OF THE DISCLOSURE

An apparatus and method of implementing a circuit representing a complex polynomial equation in a hardware description language (HDL) for implementing an ASIC (Application Specific Integrated Circuit) is provided. A serial circuit representing the complex polynomial equation is implemented in a software program. The serial circuit implementation is simulated to produce a plurality of parallel equations that are mapped into HDL with ASCII strings. In one embodiment, the complex polynomial equation is a Bose-Chaudhuri-Hocquenghem (BCH) code utilized in forward error correction circuitry.

APPENDIX A